What is claimed is:

1. A scanning circuit, comprising:

a plurality of transfer stages connected in series, each of which receives an input signal and produces a corresponding output signal in response to a clock signal;

an output circuit which logically combines the output signals of said transfer stages with another signal to generate scanning pulses; and

a clock generating circuit that supplies clock signals to said transfer stages in an alternating manner to generate a progressive sequence of scanning pulses.

2. The scanning circuit of claim 1, wherein said output circuit logically combines the output signal of a given transfer stage with the input signal to said stage.

3. The scanning circuit of claim 2, wherein each transfer stage comprises a switch that receives the input signal and is activated by one of said clock signals, and a buffer for receiving and holding the input signal when said switch is closed.

4. The scanning circuit of claim 2, wherein said output circuit performs a logical AND function of the input and output signals of each transfer stage, respectively.

5. The scanning circuit of claim 2, wherein said transfer stages are divided into two groups, one of which comprises odd-numbered stages of said series and the other of which comprises even-numbered stages of said series, and wherein said clock generating circuit supplies clock pulses to said two groups in an alternating manner.

6. The scanning circuit of claim 1, wherein said transfer stages are divided into three groups, wherein one group comprises each of the transfer stages at the 3m-2 ordinal position in said series, where m=1,2,3..., a second group comprises each of the transfer stages at the 3m-1 ordinal position in said series, and the third group comprises each of the transfer stages at the 3m ordinal position in said series, and wherein said clock generating circuit supplies clock pulses to said three groups in a sequential manner.

7. The scanning circuit of claim 6, wherein said output circuit logically combines the input signal of the k-th transfer stage in said series with the output signal of the (k+1)-th transfer stage in said series.

8. The scanning circuit of claim 7, wherein said output circuit performs a logical AND function of the input and output signals of said k-th and (k+1)-th stages, respectively.

9. The scanning circuit of claim 6, wherein each transfer stage comprises a switch that receives the input signal and is activated by one of said clock signals, and a buffer for receiving and holding the input signal when said switch is closed.

10. The scanning circuit of claim 1, wherein said transfer stages are divided into two groups, one of which comprises odd-numbered stages of said series and the other of which comprises even-numbered stages of said series, and wherein said clock generating circuit supplies clock pulses to said two groups in an alternating manner.

11. The scanning circuit of claim 10, wherein said other signal is a gate signal having two states that are synchronized with the supply of clock pulses to said two groups of transfer stages, respectively.

12. The scanning circuit of claim 11, wherein said output circuit comprises a first group of AND circuits, each having one input that receives the output signal of a corresponding one of the transfer stages in one of said groups of transfer stages, and a second group of AND circuits, each having one input that receives the output signal of a corresponding one of the transfer stages in the other group of transfer stages.

13. The scanning circuit of claim 12, wherein the AND circuits in said first group have a second input that receives a first gate signal, and the AND circuits in said second group have a second input that receives a second gate signal that is complementary to said first gate signal.

14. The scanning circuit of claim 1, wherein said plurality of transfer stages comprises:

a first group of transfer stages connected in series, wherein each transfer stage of said first group includes a first switch for receiving an input signal, a first inverter for receiving signals passed by said first switch, a second switch for receiving signals from said first inverter, and a second inverter for receiving signals passed by said second switch; and

a second group of transfer stages connected in series, wherein each transfer stage of said second group includes a third group of transfer stages connected in series, wherein each transfer stage of said third group includes a third switch for receiving an input signal, a third inverter for receiving signals passed by said third switch, a fourth switch for receiving signals from said third inverter, and a fourth inverter for receiving signals passed by said fourth switch.

15. The scanning circuit of claim 14, wherein said output circuit comprises a sequence of AND circuits, each of which has one input that receives the output signal from a corresponding one of the transfer stages in said first group, and a second input that receives the output signal from a corresponding one of the transfer stages in said second group.

16. The scanning circuit of claim 15, wherein each AND circuit at the 2m-1 ordinal position in said sequence, where m=1,2,3..., is connected to the m-th transfer stage in said first group and the m-th transfer stage in said second group, and each AND circuit at the 2m ordinal position in said sequence is connected to the (m+1)-th transfer stage in said first group and the m-th transfer stage in said second group.

17. The scanning circuit of claim 14, wherein said clock generating circuit supplies first and second clock pulses in an alternating manner, wherein said first clock pulses are applied to said first and fourth switches, and said second clock pulses are applied to said second and third switches.

18. A scanning circuit, comprising:

a plurality of transfer stages connected in series, each of which includes a switch that receives an input signal in response to a clock signal, and that produces an output signal having a state related to said input signal;

a clock generating circuit that generates a first clock signal at a given frequency having a first phase that is applied to the switches in a first group of said transfer stages, to cause said transfer stages to receive an input signal at a time corresponding to said first phase, and a second clock signal at said given frequency having a second phase different from said first phase, that is applied to the switches in a second group of said transfer stages, to cause said transfer stages in

said second group to receive an input signal at a time corresponding to said second phase; and

an output circuit comprising a sequence of AND gates, each of which receives an output signal from a transfer stage in said first group and a transfer stage in said second group, to produce a sequence of scanning pulses at a frequency higher than said given frequency.

19. The scanning circuit of claim 18, wherein the transfer stages of said first group and the transfer stages of the second group are connected in series in an alternating manner, such that the output signal of a transfer stage in one group is the input signal of a transfer stage in the other group.

20. The scanning circuit of claim 18, wherein said clock generating circuit generates a third clock signal at said given frequency having a third phase different from said first and second phases, that is applied to the switches in a third group of said transfer stages.

21. The scanning circuit of claim 18, wherein the transfer stages of said first group are connected to one another in a first series such that the output signal of one transfer stage in said first group is the input signal of another transfer stage in said first group, and the transfer stages of said second group are connected to one another in a second series such that the output signal of one transfer stage in said second group in the input signal to another transfer stage in said second group.

22. The scanning circuit of claim 21, wherein each AND circuit at the 2m-1 ordinal position in said sequence, where m=1,2,3..., is connected to the m-th transfer stage in said first group and the m-th transfer stage in said second group, and each AND circuit at the 2m ordinal position in said sequence is

connected to the (m+1)-th transfer stage in said first group and the m-th transfer stage in said second group.

23. The scanning circuit of claim 21, wherein each transfer stage of said first group includes a first switch for receiving an input signal, a first inverter for receiving signals passed by said first switch, a second switch for receiving signals from said first inverter, and a second inverter for receiving signals passed by said second switch; and each transfer stage of said second group includes a third switch for receiving an input signal, a third inverter for receiving signals passed by said third switch, a fourth switch for receiving signals from said third inverter, and a fourth inverter for receiving signals passed by said fourth switch.

24. The scanning circuit of claim 23, wherein said first clock signal is applied to said first and fourth switches, and said second clock signal is applied to said second and third switches.

25. A scanning circuit, comprising:

a plurality of transfer stages connected in series, each of which includes a switch that receives an input signal in response to a clock signal, and produces an output signal having a state related to said input signal;

a clock generating circuit that generates a first clock signal at a given frequency having a first phase that is applied to the switches in a first group of said transfer stages, to cause said transfer stages to receive an input signal at a time corresponding to said first phase, and a second clock signal at said given frequency having a second phase different from said first phase, that is applied to the switches in a second group of said transfer stages, to cause said transfer stages in said second group to receive an input signal at a time corresponding to said second phase; and

an output circuit including:

a first group of AND gates each having a first input that receives the output signal from a corresponding one of the transfer stages in said first group of transfer stages and a second input that receives a first gating signal that is synchronized with said first clock signal, so that said AND gates in said first group are activated when said first clock signal is applied to the switches in said first group of transfer stages; and

a second group of AND gates each having a first input that receives the output signal from a corresponding one of the transfer stages in said second group and a second input that receives a second gating signal that is synchronized with said second clock signal, so that said AND gates in said second group are activated when said second clock signal in applied to the switches in said second group of transfer stages.

26. The scanning circuit of claim 25, wherein said first and second gating signals are complementary to one another.

27. An imaging apparatus, comprising:

an image sensing device having an array of pixels;

an output circuit for outputting values from selected pixels in said array;

a scanning circuit for selecting the pixels in said array, including a plurality of transfer stages connected in series, each of which receives an input signal and produces a corresponding output signal in response to a clock signal, and an output circuit which logically combines the output signals of said transfer stages with another signal to generate scanning pulses; and

a clock generating circuit that supplies clock signals to said transfer stages in an alternating manner to generate a progressive sequence of scanning pulses.

28. A scanning circuit, comprising:

a plurality of transfer stages connected in series, each of which includes a switch that receives an input signal in response to a clock signal, and produces an output signal having a state related to said input signal;

a clock generating circuit that generates a first clock signal at a given frequency having a first phase that is applied to the switches in a first group of said transfer stages, to cause said transfer stages to receive an input signal at a time corresponding to said first phase, a second clock signal at said given frequency having a second phase different from said first phase, that is applied to the switches in a second group of said transfer stages, to cause said transfer stages in said second group to receive an input signal at a time corresponding to said second phase, and a third clock signal at said given frequency having a third phase different from said first and second phases, that is applied to the switches in a third group of said transfer stages, to cause said transfer stages in said third group to receive an input signal at a time corresponding to said third phase; and

an output circuit comprising a sequence of AND gates, each of which receives an output signal from a transfer stage in one of said groups and an output signal from a transfer stage in another one of said groups, to produce a sequence of scanning pulses at a frequency higher than said given frequency.

29. The scanning circuit of claim 28, wherein the transfer stages of said first, second and third groups are connected in series in a cyclical manner, such that the output signal of a transfer stage in the first group is the input signal of a transfer stage in the second group, the output signal of a transfer stage in the second group is the input signal of a transfer stage in the third group, and the output signal of a transfer stage in the third group is the input signal of a transfer stage in the first group.

30. The scanning circuit of claim 29, wherein each AND gate of said output circuit receives the input signal of a given transfer stage and the output signal of the next transfer stage which immediately follows said given stage in said series.

31. A pulse signal generating apparatus comprising:

a transfer stage portion comprising a plurality of transfer stages connected in series, said transfer stages each including at least one switch for passing current in a direction in which the transfer stages are connected in series;

a first pulse generating portion that supplies a first driving pulse to first switches in the transfer stage portion at predetermined intervals;

a second pulse generating portion that supplies a second driving pulse whose phase is shifted from that of the first driving pulse, at the predetermined intervals, to second switches of the transfer stages which switches are not included in the first switches; and

an output portion that outputs pulse signals successively from a plurality of gates connected to the transfer stages, at intervals shorter than the predetermined intervals.

32. The pulse signal generating apparatus of claim 31 wherein:

the gates comprise first gates capable of outputting pulse signals by being supplied with the first driving pulse, and second gates capable of outputting pulse signals by being supplied with the second driving pulse; and

a pulse signal for scanning is output alternatively from a gate included in the first gates and a gate included in the second gates.